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A 6 WATT POWER GaAs FET FOR 14.0-14.5GHz BAND

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ABSTRACT

An internally matched GaAs FET with output power above 38dBm(6.3W) and linear power gain above 5.8dB has been developed for the 14.0-14.5GHz band. These results were achieved by using high quality GaAs wafers prepared by molecular beam epitaxy (MBE) and optimizing the channel recess structure.

Additionally, the package size of the FET was successfully reduced by using a high dielectric substrate for the internal matching circuits of both input and output.

INTRODUCTION

In recent years high power GaAs FETs have been developed for the substitution of the traditional TWT amplifier (1), (2), (3). Such high power GaAs FETs with high performance have been in great demand for variety of applications. Especially, satellite business communication systems(SBSs) using VSAT(Very Small Aperture Terminal), operating at Ku-band(14/12 GHz), are expected to become a large market. In order to apply the GaAs FETs in this system, small-sized GaAs FETs with high power and high gain are required from a standpoint of minimizing the size of the antenna and other equipments.

This paper describes the results of the high power GaAs FETs development using small-sized package. Using MBE material and optimizing the channel recess structure, high performance FETs were fabricated. Then FET chips were internally matched by the quasi-distributed circuits that were constructed on the high dielectric constant substrate. By combining two FET chips, an output power of 7.1W was achieved at 14.3GHz.

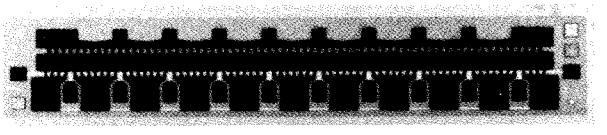

Fig.1 A photograph of the GaAs FET chip.

DEVICE FABRICATION

In order to obtain high output power above 3W from one FET chip, the total gate width was designed to be 10.5mm. For gain improvement in the high frequency range, it is important to optimize the unit gate width as well as the gate length. However, as the unit gate width shortens, the number of gate fingers increases to get the same total gate width. It causes the deterioration of RF performance because FET chip can not operate uniformly in phase on the large chip. Consequently, the gate length and the unit gate width were chosen 0.5μm and 75μm respectively.

The top view of the designed FET chip is shown in Fig.1. The chip size is 0.5mm x 2.5mm.

Epitaxial layers grown by molecular beam epitaxy (MBE) were used to achieve high performance and to get better uniformity in a wafer. The best thickness of the active layer was found to be around 0.3μm in order to optimize the channel recess structure. The carrier concentration of the active layer was $2\times10^{17}/cm^3$.

Via hole and air-bridge structures were used to reduce source inductance, thermal resistance and parasitic capacitance. The FET chip was thinned down to 30μm thick by chemical etching, and gold plated heat-sink of 30μm thick was formed on the backside of the FET chip.

INTERNAL MATCHING

The fabricated FET chips were internally matched in the hermetically sealed package. The input and output matching circuits consisted of two open-stub lines connected by some high impedance transmission lines. These circuits were considered to be quasi-distributed lines. The circuits were constructed on high dielectric constant substrate($\varepsilon r=38$) of 0.2mm thickness. No other substrates were required in order to

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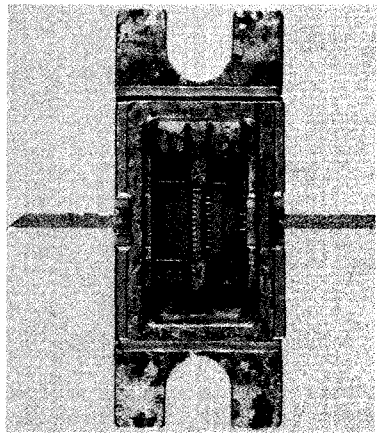

Fig.2 An inner view of the 1-chip device.

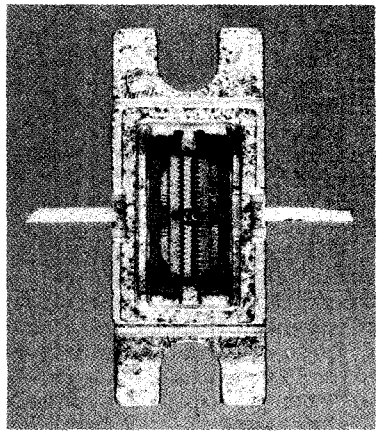

Fig.3 An inner view of the 2-chip device.

match the impedance of the FET to 50 ohm. This construction made it possible to reduce device size and to adjust the impedance of circuits to 50 ohm easily. Accordingly the package size was also reduced to 6.5mm x 12mm.

Fig.2 shows an inner view of an internally matched GaAs FET for 1-chip. The size of substrate for matching circuit is 1.4mm x 3.1mm.

Fig.3 shows an inner view of the internally matched GaAs FET constructed by combining 2 chips. The matching circuits of this 2-chip device were composed of the same high dielectric substrate as 1-chip device.

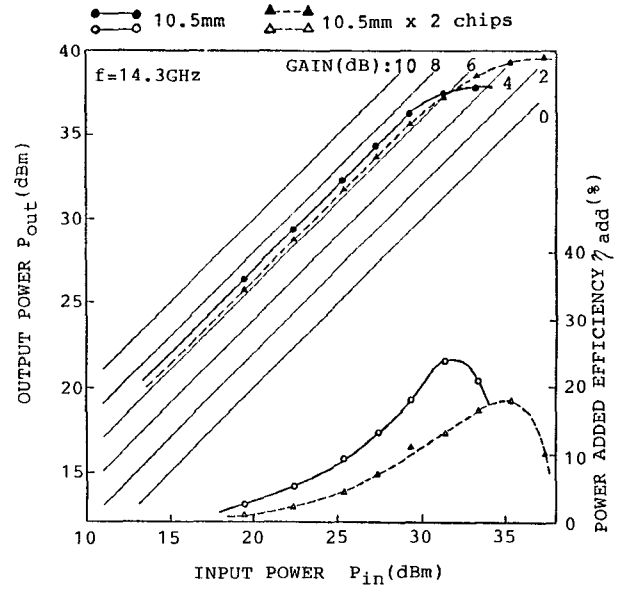

Fig.4 Input power versus output power at 14.3GHz for the 1-chip and 2-chip devices.

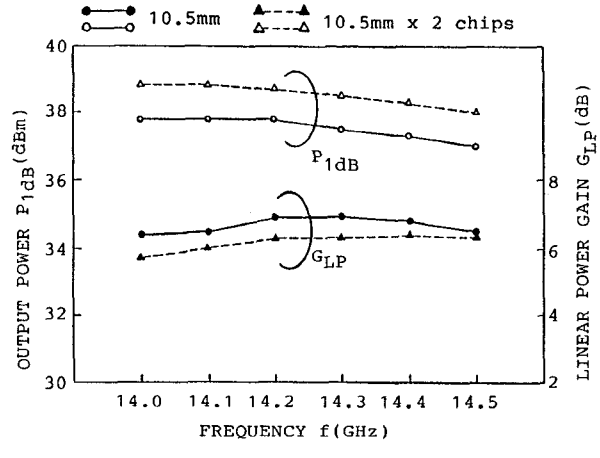

Fig.5 Output power and linear power gain versus frequency for the 1-chip and 2-chip devices.

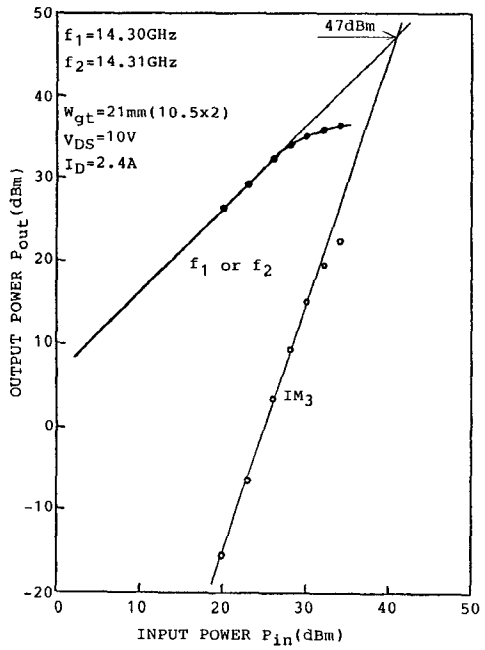

Fig.6 Third-order intermodulation characteristic of the 2-chip device.

PERFORMANCE

RF performances were tested under the bias conditions of V_{DS}=10V, I_D=1.2A for the 1-chip device, and V_{DS}=10V, I_D=2.4A for the 2-chip device.

Fig.4 shows output power (Pout) and power added efficiency (ηadd) vs. input power (Pin) of the 1-chip and 2-chip devices. At 14.3GHz, the 1-chip device had a linear power gain of 6.9dB, an output power of 37.5dBm(5.6W) and a power added efficiency of 24.6% at 1dB gain compression. The output power per gate width was 0.52W/mm. This is the largest output power per gate width in the 14.0-14.5GHz band. In the 2-chip device, the linear power gain was 6.3dB, the output power was 38.5dBm(7.1W) and the power added efficiency was 17.8%. These results were obtained without additional tuning.

Fig.5 shows the gain and output power characteristics of the 1-chip and 2-chip devices in the 14.0-14.5GHz band. The 1-chip device achieved linear power gain above 6.4dB and output power above 37dBm(5W) at 1dB gain compression over the frequency range of 14.0-14.5GHz. The 2-chip device realized linear power gain above 5.8dB and output power above 38dBm(6.3W). The output power of 2-chip device is small compared with the expectant value from 1-chip device because of the unbalanced operation in the combined chips. The RF performance of 2-chip device will be improved further by optimization of the internal matching circuits.

The third order intermodulation characteristic was measured by two tone test. The result of the 2-chip device is shown in Fig.6. At 37dBm output power, IM3 was 22dBc. The intercept point was +47dBm. This value is sufficient for use in VSAT.

CONCLUSION

Using MBE material and optimizing the channel recess structure, high power FETs with output power above 5W per one chip were realized. The output power per gate width was 0.52W/mm. By combining two chips, a 6W power GaAs FET for the 14.0-14.5GHz band has been developed. This high power GaAs FET is suitable for use in satellite business communication systems. This 6W power GaAs FET is expected to contribute to the realization of small size Solid State Power Amplifier (SSPA) with high output power suitable for VSAT.

ACKNOWLEDGMENT

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